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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,198	07/02/2001	K. Paul Muller	YO999-247DIV	1509

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EXAMINER	
TRINH, HOA B	

ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
08/03/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/895,198	MULLER ET AL.	
	Examiner	Art Unit	
	HOA B. TRINH	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *45-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *45-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. An amendment filed on 03/30/2009 has been considered. New claims 45-59 are pending in this application.

Claim Objections

2. Claims 46, 51, 56 are objected to because of the following informalities: In each of the claim, "a face" should be deleted. Appropriate correction is required.

3. Claims 49, 59 are objected to because of the following informalities: In each of the claims, a term "coplanar" is vague and ambiguous, because the claimed elements that are intersected are not supposed to be coplanar. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 45-59 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker (5,662,768; reference of record cited on 04/12/2002).

Regarding claim 45, in figure 3, Rostroker discloses an integrated circuit structure comprising: a substrate 4 having an upper surface, wherein said substrate 4 comprises a substrate material; an opening 32 in said upper surface of said substrate defined by said substrate material; a second surface parallel to and at a depth less than said upper surface; a third surface parallel to and at a second depth less than said second surface; a first

vertical wall substantially orthogonal to and intersecting said upper surface at said opening and said second surface; a second vertical wall substantially orthogonal to and intersecting said second and said third surfaces; and a conductor 30 filling said opening, wherein said second vertical wall is positioned in a vertical direction within a horizontal dimension of said opening 32. see marked-up figure 3 below.

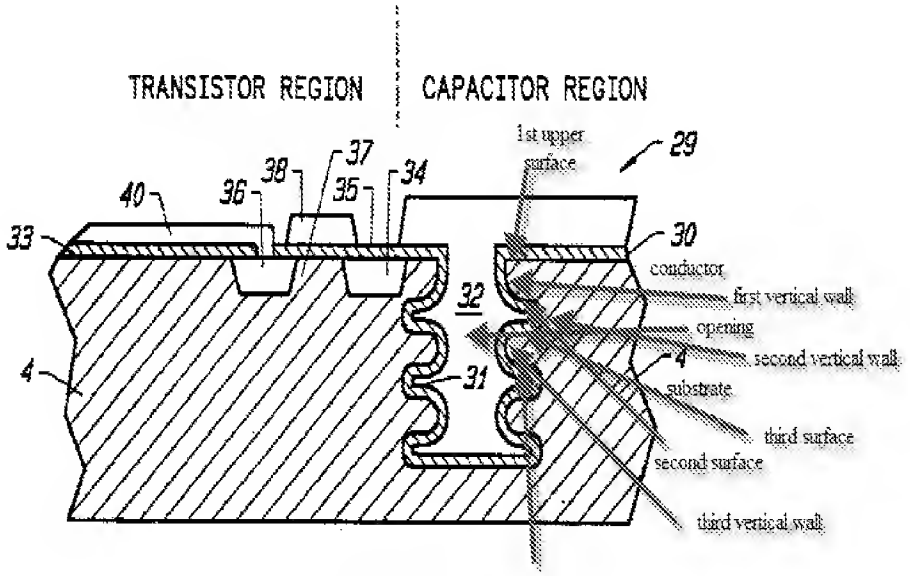

FIG. 3

Regarding claim 46, said second surface is positioned in an upward direction. See marked-up figure 3.

Regarding claim 47, first and second vertical walls are symmetrically disposed from said first and second vertical walls on an opposite side of a centerline of said opening 32. See marked-up figure 3.

Regarding claim 48, said upper, second and third surfaces each intersect their respective first and second vertical walls at substantially right angles. See marked-up figure 3.

Regarding claim 49, as best understood, an intersection of said second vertical wall and said second surface is coplanar in a horizontal direction with an intersection of said second vertical wall and said third surface. See marked-up figure 3.

Regarding claim 50, in figure 3, Rostroker discloses an integrated circuit structure comprising: a substrate 4 having an upper surface, wherein said substrate 4 comprises a substrate material; an opening 32 in said upper surface of said substrate 4 defined by said substrate material; a second surface parallel to and at a depth less than said upper surface; a third surface parallel to and at second depth less than said second surface; a fourth surface parallel to and at a third depth less than said third surface; a first vertical wall substantially orthogonal to and intersecting said upper surface at said opening and said second surface; a second vertical wall substantially orthogonal to and intersecting said second and said third surfaces; a third vertical wall substantially orthogonal to and intersecting said third and fourth surfaces; and a conductor 30 filling said opening 32, wherein said second vertical wall is positioned in a vertical direction within a horizontal dimension of said opening 32, and wherein said third vertical wall is positioned vertically between a horizontal dimension of said opening and said second vertical wall. See marked-up figure 3.

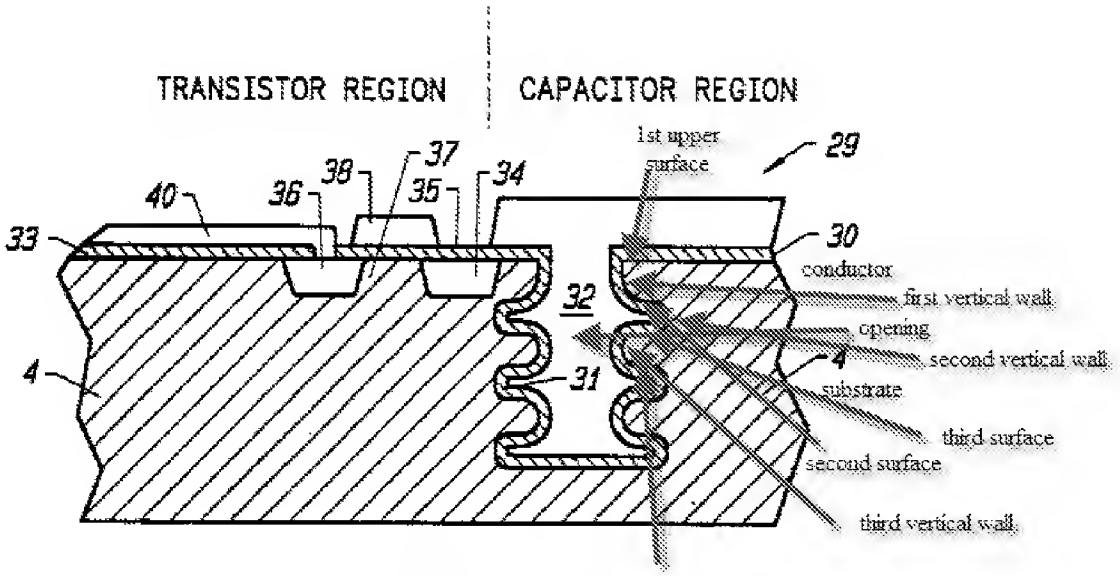

FIG. 3

Regarding claim 51, said second and fourth surfaces are positioned in an upward direction. See marked-up figure 3.

Regarding claim 52, said third surface is positioned in a downward direction. See marked-up figure 3.

Regarding claim 53, corresponding first, second and third vertical walls are symmetrically disposed from said first and second vertical walls on an opposite side of a centerline of said opening. See marked-up figure 3.

Regarding claim 54, said upper, second, third and fourth surfaces each intersect their respective first, second and third vertical walls at substantially right angles. See marked-up figure 3.

Regarding claim 55, Rostroker discloses an integrated circuit structure comprising:

a substrate having an upper surface, wherein said substrate comprises a substrate material

an opening in said upper surface of said substrate defined by said substrate material; a second surface parallel to and at a depth less than said upper surface; a third surface parallel to and at a second depth less than said second surface; a first vertical wall substantially orthogonal to and intersecting said upper surface at said opening and said second surface; a second vertical wall substantially orthogonal to and intersecting said second and said third surfaces; and a conductor filling said opening, and

wherein said second vertical wall is positioned in a vertical direction within a horizontal dimension of said opening. See marked-up See marked-up figure 3.

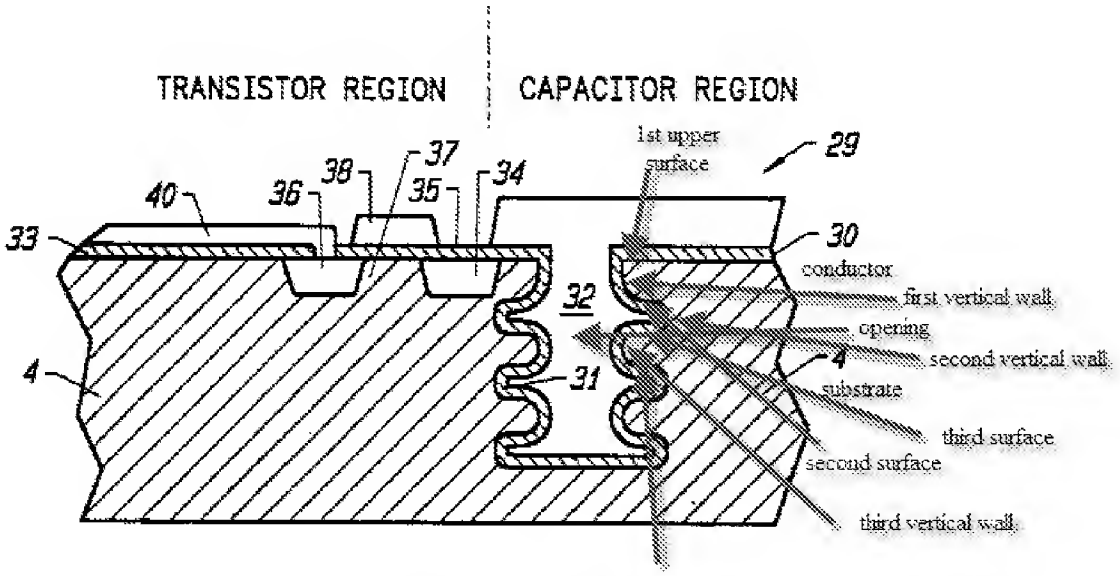

FIG. 3

Regarding claim 56, said second surface is positioned in a downward direction. See marked-up figure 3.

Regarding claim 57, corresponding first and second vertical walls are symmetrically disposed from said first and second vertical walls on an opposite side of a centerline of said opening. See marked-up figure 3.

Regarding claim 58, said upper, second and third surfaces each intersect their respective first and second vertical walls at substantially fight angles. See marked-up figure 3.

Regarding claim 59, as best understood, a intersection of said second vertical wall and said second surface is coplanar in a horizontal direction with an intersection of said second vertical wall and said third surface. See marked-up figure 3.

Response to Arguments

1. Applicant's arguments with respect to the new claims have been considered but they are moot in view of the new rejection.

In the new claims, applicant does not recite the rectangular portion or any dimension as alleged in the argument on page 7. Rostroker discloses the limitation of the new claims 45 and 55 in figure 3. see the marked-up figure 3 and the rejection above.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to (Vikki) Hoa B. Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Ms. Davienne Monbleau, can be reached at (571) 272-1945. The office fax number is 571-273-8300.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see **http://pair-direct.uspto.gov**. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications have ceased to be mailed to applicants with Office actions since June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (**www.uspto.gov**), from the Office of Public Records and from

commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy.

Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

/(Vikki) Hoa B Trinh/
Examiner, Art Unit 2893

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893